

CLAIMS

What is claimed is:

1. A process for providing electrical connection, comprising:  
providing a semiconductor die receiving member that is configured to receive a semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:  
a plurality of first contact sites configured to lie underneath said semiconductor die when said semiconductor die is proximate said die receiving member; and  
a plurality of second contact sites configured to lie adjacent said semiconductor die when said semiconductor die is proximate said die receiving member, each first contact site of said plurality of first contact sites being in electrical connection with an adjacent second contact site of said plurality of second contact sites;  
providing said semiconductor die, wherein said semiconductor die includes a first face, an opposite second face, and a plurality of bond pads on said first face configured for flip-chip mounting or wirebonding; and  
mounting said semiconductor die onto said semiconductor die receiving member in one of:  
flip chip mounting, wherein said flip-chip mounting comprises:  
disposing said first face proximate said die receiving member;  
and  
electrically connecting each of said plurality of bond pads with a corresponding first contact site of said plurality of first contact sites; and

1 wirebonding, wherein said wirebonding comprises:

2 disposing said second face proximate said die receiving  
3 member; and

4 electrically connecting each of said plurality of bond pads  
5 with a corresponding second contact site of said plurality of second  
6 contact sites.

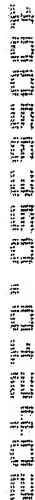
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8 2. The process of claim 1, wherein electrically connecting each of said plurality  
9 of bond pads comprises placing conductive material between each of said plurality of bond  
10 pads and said plurality of first contact sites, or attaching wiring between each of said  
11 plurality of bond pads and said plurality of second contact sites.

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13 3. The process of claim 1, further comprising, after electrically connecting each  
14 of said plurality of bond pads, applying an adhesive underfill between said first or second  
15 face and said die receiving member.

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17 4. The process of claim 1, wherein said wirebonding further comprises, prior to  
18 disposing said second face proximate said die receiving member, providing an adhesive layer  
19 on said die receiving member.

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21 5. The process of claim 1, further comprising placing said semiconductor die  
22 receiving member in electrical connection with external circuitry.

23  
24 6. The process of claim 5, wherein said external circuitry is a motherboard.



1           7.     A process for providing electrical connection, comprising:

2                 providing a semiconductor die having a first face, a second face opposite said  
3                 first face, a periphery, and a plurality of bond pads arrayed on said first face and  
4                 configured for flip-chip mounting or wirebonding;

5                 providing a semiconductor die receiving member configured to receive a  
6                 respective semiconductor die which can be mounted either through flip-chip  
7                 mounting or wirebonding, the die receiving member comprising:

8                         a die receiving surface having a die receiving region bounded by a  
9                         perimeter which corresponds to and is defined by said periphery of said  
10                         semiconductor die, said die receiving region being configured so as to receive  
11                         said semiconductor die;

12                         a package mount surface;

13                         a plurality of first contact sites positioned on said die receiving  
14                         surface substantially within said perimeter, each of said first contact sites  
15                         corresponding to one of said bond pads;

16                         a plurality of second contact sites positioned on said die receiving  
17                         surface substantially outside of said perimeter, each of said second contact  
18                         sites corresponding to one of said bond pads;

19                         a plurality of terminal contact sites on said package mount surface;  
20                         and

21                         a plurality of electrically conductive traces, each electrically  
22                         conductive trace corresponding to one of said terminal contact sites, one of  
23                         said first contact sites, and one of said second contact sites which is adjacent  
24                         to said one of said first contact sites, and providing electrical connection  
25                         therebetween; and  
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1           10.   The process of claim 7, further comprising:  
2                providing a mounting substrate having a plurality of contact pads; and  
3                mounting said semiconductor die receiving member over said mounting  
4                substrate, including:

5                    positioning said semiconductor die receiving member over said  
6                    mounting substrate such that said package mount surface is disposed over  
7                    said mounting substrate; and

8                    establishing electrical connection between each of said terminal  
9                    contact sites and one of said contact pads that corresponds thereto.

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11           11.   The process of claim 10, wherein positioning said semiconductor die  
12           receiving member over said mounting substrate comprises aligning said semiconductor die  
13           receiving member such that said die receiving surface is substantially orthogonal to said  
14           mounting substrate.

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16           12.   The process of claim 10, wherein positioning said semiconductor die  
17           receiving member over said mounting substrate comprises aligning said semiconductor die  
18           receiving member such that said die receiving surface is substantially parallel to said  
19           mounting substrate.

13. A process for providing electrical connection, comprising:

providing a semiconductor die receiving member that is configured to receive a semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a plurality of first contact sites configured to lie underneath said semiconductor die when said semiconductor die is proximate said die receiving member; and

a plurality of second contact sites configured to lie adjacent said semiconductor die when said semiconductor die is proximate said die receiving member, each first contact site of said plurality of first contact sites being in electrical connection with an adjacent second contact site of said plurality of second contact sites;

providing said semiconductor die, wherein said semiconductor die includes a first face, an opposite second face, and a plurality of bond pads on said first face configured for flip-chip mounting or wirebonding;

wirebonding said semiconductor die onto said semiconductor die receiving member in an orientation wherein each of said bond pads is in electrical connection with a second contact site of said plurality of second contact sites, wherein said wirebonding comprises:

providing an adhesive layer on said die receiving member;

disposing said second face proximate said die receiving member; and

electrically connecting each of said plurality of bond pads with a corresponding second contact site of said plurality of second contact sites using wiring; and

placing said semiconductor die receiving member in electrical connection with a motherboard.

14. A process for providing electrical connection, comprising:

providing a semiconductor die having a first face, a second face opposite said first face, a periphery, and a plurality of bond pads arrayed on said first face and configured for flip-chip mounting or wirebonding;

providing a semiconductor die receiving member configured to receive a respective semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a die receiving surface having a die receiving region bounded by a perimeter which corresponds to and is defined by said periphery of said semiconductor die, said die receiving region being configured so as to receive said semiconductor die;

a package mount surface;

a plurality of first contact sites positioned on said die receiving surface substantially within said perimeter, each of said first contact sites corresponding to one of said bond pads;

a plurality of second contact sites positioned on said die receiving surface substantially outside of said perimeter, each of said second contact sites corresponding to one of said bond pads;

a plurality of terminal contact sites on said package mount surface;  
and

a plurality of electrically conductive traces, each electrically conductive trace corresponding to one of said terminal contact sites, one of said first contact sites, and one of said second contact sites which is adjacent to said one of said first contact sites, and providing electrical connection therebetween;

1 mounting said semiconductor die onto said die receiving region, said  
2 semiconductor die being mounted according to one of:

3 a flip-chip mounting process including:

4 disposing said first face onto said die receiving region;

5 electrically connecting each bond pad to said first contact site  
6 that corresponds thereto, wherein a conductive material is interposed  
7 between each bond pad and said first contact site that corresponds  
8 thereto; and

9 applying an adhesive underfill between said first face and said  
10 die receiving region; and

11 a wirebonding process including:

12 disposing said second face onto said die receiving region; and

13 electrically connecting each bond pad to said second contact  
14 site that corresponds thereto;

15 providing a mounting substrate having a plurality of contact pads; and

16 mounting said semiconductor die receiving member over said mounting  
17 substrate, including:

18 positioning said semiconductor die receiving member over said  
19 mounting substrate such that said package mount surface is disposed over  
20 said mounting substrate, wherein said semiconductor die receiving member  
21 is aligned such that said die receiving surface is substantially orthogonal to  
22 said mounting substrate; and

23 establishing electrical connection between each of said terminal  
24 contact sites and one of said contact pads that corresponds thereto.  
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